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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,743	11/21/2003	Bernard J. New	X-1141 US	3152

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,743	NEW ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-26* is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/14/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment received on 2/14/2005 has been reviewed and considered with the following results:

As to the objection to the drawings, Applicant's revision of the drawings has overcome the objection, as such; the objection has been withdrawn.

As to the rejections to the claims, under 35 U.S.C. 112, 1st and 2nd paragraphs, Applicant's amendment and clarification have overcome the rejections, as such; the rejections have been withdrawn.

The prior art rejections to the claims made in the previous Office Action, mailed on 11/18/04, are now withdrawn in view of Applicant's amendments and arguments, the arguments have been considered but are moot in view of a new action on the merits appears below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 8, 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (US Pat. 6,275,079; previously cited) in view of Trimberger et al. (US Pat. 5,811,985).

With regard to claim 1, Park discloses in Figs. 4-7 a delay locked loop comprising a primary delay line (103') that comprises a plurality of series-connected delay elements; and a

delay control circuit (105) coupled to the primary delay line. Fig. 3 of Park shows a delay locked loop meeting all of the claimed limitations except for using a memory cell (220 in instant Fig. 2) as a control signal of multiplexer. Trimberger et al. teaches in Fig. 6 a multiplexer (235) controlled by a memory cell (280) for selecting one of the input signals. Therefore, it would have been obvious to one of ordinary skill in the art to implement the memory cell, as the control signal, taught by Trimberger et al. with the prior art (Figs. 4-7 of Park) for the advantage of easily changing the selected input by using the programmable memory cell.

With regard to claims 2, 3, 5, 6, 8, and 9, the references also meet the recited limitations in these claims.

With regard to claim 4, the above discussed that the delay locked loop of Park meets all of the claimed limitations except for the limitation that the first voltage (Vpp) is 10 or more percent greater than the second voltage (Vcc). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to set the first voltage (Vpp) is at a certain percent greater than the second voltage, including 10 or more percent, to meet the specific condition of the particular application. It has been held that discovering an optimum range or to optimally match to an application is obvious to the skilled artisan. See *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

With regard to claim 15, the delay locked loop of Park further comprises an inherent voltage regulator for providing at least one of the first and second voltages (Vpp, Vcc).

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Trimberger et al., as applied to claims 1, 2, and 5 above; and further in view of Krishnamurthy (US Pat. 6,271,713; previously cited).

The above discussed that the delay locked loop, and the method of use thereof, of the references meets all of the claimed limitations except for the limitation that each of the inverters (205_1 - 205_N in instant Fig. 2) comprises a transistor having a well region coupled to the voltage distribution line (222). Krishnamurthy teaches in Fig. 4 a circuit having each of the inverters (152, 154) comprises a transistor (M2, M4) having a well region coupled to the voltage distribution line (116). Therefore, it would have been obvious to one of ordinary skill in the art to implement that teaching with the prior art in order to improve the switching speed of the circuit.

5. Claims 1, 2, and 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dortu et al. (US Pat. 6,252,443) in view of Park, and further in view of Trimberger et al.

With regard to claim 1, Dortu et al. discloses in Fig. 10 a delay locked loop comprising a primary delay line (112') comprising a plurality of series-connected delay elements. Fig. 10 of Dortu et al. shows a delay locked loop meeting all of the claimed limitations except for a delay control circuit (213 in instant Fig. 2). Park teaches in Fig. 7 a delay locked loop circuit having a delay control circuit (702) coupled to the primary delay line (103) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art to implement the delay control circuit taught by Park with the prior art (Fig. 10 Dortu et al.) for the advantage of setting the delay line at desired pre-determined time delay. Furthermore, Trimberger et al. teaches in Fig. 6 a multiplexer (235) controlled by a memory cell (280) for selecting one of the input signals. Therefore, it would have been obvious to one of ordinary skill in the art to implement the memory cell, as the control signal, taught by Trimberger et al. with the prior arts for the advantage of easily changing the selected input by using the programmable memory cell.

With regard to claims 2 and 15, the references also meet the recited limitations in these claims.

With regard to claim 10, the delay locked loop further comprises a clock input terminal (Input) for receiving an input clock signal (Ckin); a first multiplexer (115s in the top row) coupled to receive delayed versions of the input clock signal from the delay elements of the primary delay line; and a delay selection circuit (114) coupled to control the first multiplexer in response to the input clock signal and a distributed version of the input clock signal.

With regard to claim 11, the delay locked loop further comprises a second multiplexer (115s in the second row) having a first input terminal coupled to receive a delayed version of the input clock signal routed by the first multiplexer (one of plurality of 115s in the top row); and a fast delay element having an input terminal coupled to receive the delayed version of the input clock signal routed by the first multiplexer, and an output terminal coupled to a second input terminal of the second multiplexer (one of plurality of 115s in the second row).

With regard to claims 12 and 13, the references also meet the recited limitations in these claims.

With regard to claim 14, the above discussed circuit of the references meets all of the claimed limitations except for a clock distribution network (103 in instant Fig.1). However, it is notoriously well known in the art that clock distribution network is employed to distribute the output clock to other circuits. Therefore, it would have been obvious to one of ordinary skill in the art to utilize a clock distribution network with the circuit of the references in order to provide synchronize clocks to the subsequent circuits, and the feedback clock can be either the output clock of the multiplexer or from the clock distribution network (see Figs. 3 & 4 of Yamazaki, US

patent 5,999,027) for the advantage of providing the synchronize clock signal to meet a specific requirement which is in each case optimally matched to its application.

6. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA), Fig. 1 in the present application, in view of Park.

With regard to claim 16, the APA discloses in Fig. 1 a field programmable gate array (FPGA) circuit comprising an input clock terminal for receiving an input clock signal (CLK_IN) used to clock data into the FPGA; a global clock routing network (103) that provides a distributed clock signal (DIST_CLK) in response to the input clock signal, wherein the distributed clock signal is used to clock data into or out of the FPGA; a delay locked loop (101). Fig. 1 of APA shows a circuit all of the claimed limitations except for structural details of the delay locked loop. Park teaches in Figs. 3-7 a delay locked loop comprising a primary delay line (103,103') comprising a plurality of series-connected delay elements, wherein each of the delay elements operates in response to a voltage on a voltage distribution line (Vp); a first voltage terminal for receiving a first voltage (Vpp); a second voltage terminal for receiving a second voltage (Vcc), wherein the first voltage is greater than the second voltage; and a voltage selection circuit (702) for selectively coupling the first voltage terminal or the second voltage terminal to the voltage distribution line.

With regard to claim 17 and 18, the references also meet the recited limitations in these claims.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA), Fig. 1 in the present application, in view of Park, as applied to claims 16 and 17 above; and further in view of Krishnamurthy.

The above discussed that the FPGA circuit of the prior arts meets all of the claimed limitations except for the limitation that each of the inverters (205_1 - 205_N in instant Fig. 2) comprises a transistor having a well region coupled to the voltage distribution line (222). Krishnamurthy teaches in Fig. 4 a circuit having each of the inverters (152, 154) comprises a transistor (M2, M4) having a well region coupled to the voltage distribution line (116). Therefore, it would have been obvious to one of ordinary skill in the art to implement that teaching with the prior arts in order to improve the switching speed of the circuit.

Allowable Subject Matter

8. Claims 20-26 are allowed.

The prior art of record fails to disclose or fairly suggest a method of operating delay locked loop (200 in instant Fig. 2), having specific limitation such as a step of operating the delay elements (205_1 – 205n) in response to a first voltage (V_{S1}) when the input clock signal (CLK_IN) has a frequency greater than or equal to a first frequency; and operating the delay elements in response to a second voltage (V_{S2}) when the input clock signal has a frequency less than the first frequency, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and

Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
May 14, 2005

TUAN T. LAM
PRIMARY EXAMINER